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Interfacing of 8 Channel Optical MUX DEMUX in DWDM System

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Abstract— Purpose of this paper is to describe the hardware design interfacing of the 8 channel Optical Mux/Demux (OMD) Module in DWDM system. There are two types of OMD modules used in DWDM/CWDM system.Type-1 consists of OMD module with A/D converter and processor.Type-2 consists of OMD module without A/D converter and processor. “Multiplexing” is a term used to describe the mixing or insertion of signals into a stream; “De-multiplexing” is used to describe the removal or extraction of the signals.The communications interface between host (processor or FPGA) and OMD module is through I2C bus. The A/D converters and the EEPROM, holding module specific data, are controlled via the I2C bus and supplied with power from the DC/DC converter.

Index Terms— CWDM, DEMUX, DWDM, I2C, MUX

1 Introduction

These are passive optical filter systems which are arranged t o process specific wavelengths in and out of the transport str eam. As these are optical devices they can be used for both multiplex- ing and de-multiplexing or both. The process of filtering the wave- lengths can be performed with prisms, but morecommon tec hnolo- gies used are thin film filters, dichroic filters or interference f ilters which are used to selectively reflect a single wavelengt h of light, but pass all others transparently. Each filter is tune d for specific wavelength which is why it’s important to conn ect the correct wavelength to the correspondingI/O port. The Fig.1shows the basic function; in this example it’s a 4 port de vice with eightwavelengths on the main I/O port.Individual I /O ports will have the specific wavelength specified. COM P ort means “Common” and this is the primary single fiber I/ O connection which will contain all the multiplexed wavelen gths . This is connected to the COM port on the Optical MUX /DEMUX unit at the other end of the link.

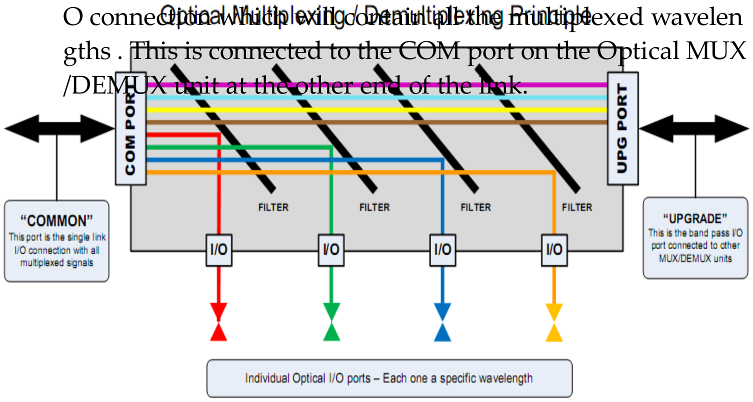

Fig.1: Block diagram of ODM system

UPG Port means “Upgrade” and this is the “pass band” p ort. To keep system costs down manufacturers offer Optical MUX/DEMUX solutions in smaller configurations which ca n be easily expanded. For example a smaller 4 port or 8 port deice rather than providing a single large 16or 18 port device . Any wavelengths present in the stream which are not supp ort- ed by thespecific optical MUX/DEMUX unit are passed on U PG port for connection to the next Optical MUX/DEMUX un it which supports these wavelengths.

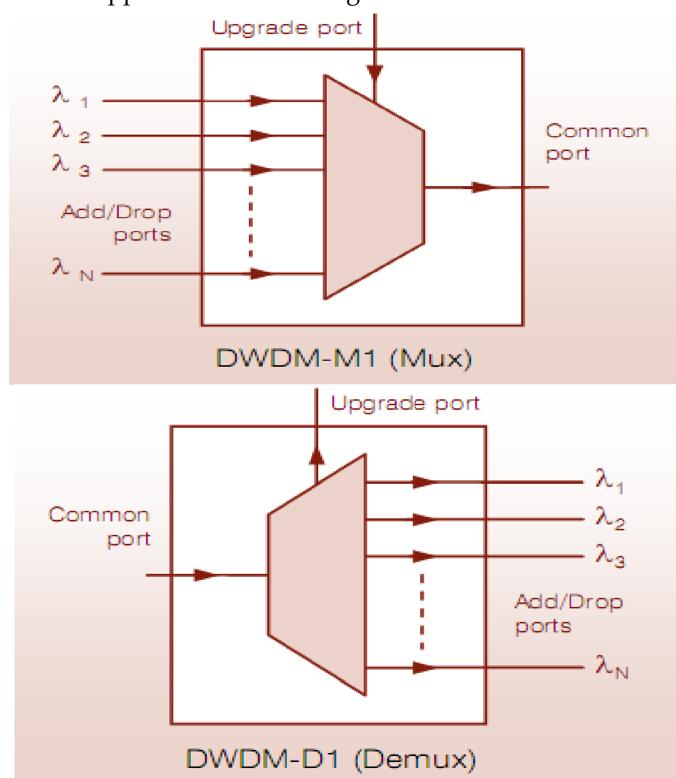

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Fig.2: Configuration of DWDM MUX/DEMUX

2 MUX AND DEMUX FUNCTIONALSCHEMATIC

The module contains an 8 channel optical multiplexer and de-multiplexer with monitoring of optical power on all input fibers (Type -2) and analog to digital (A/D) converters. (In case of Type -1). As fig.3, system uses multiplexer at the transmitter to combine the 8 input signals with optical power monitoring at the input. Channel spacing between the two operating wavelength is 20nm.

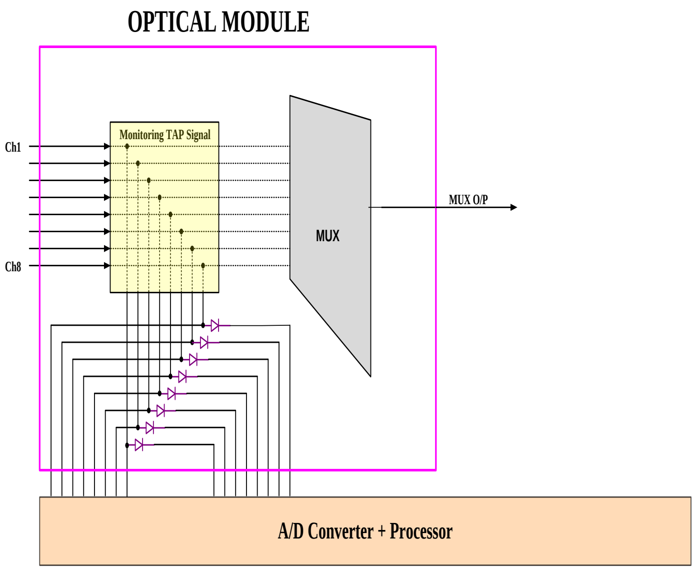

Fig.3: MUX functional schematic

As shown in the fig.4, System uses Demultiplexer at the receiver to split the combined signals (8 channels) to different operating wavelengths with channel spacing of 20nm each.

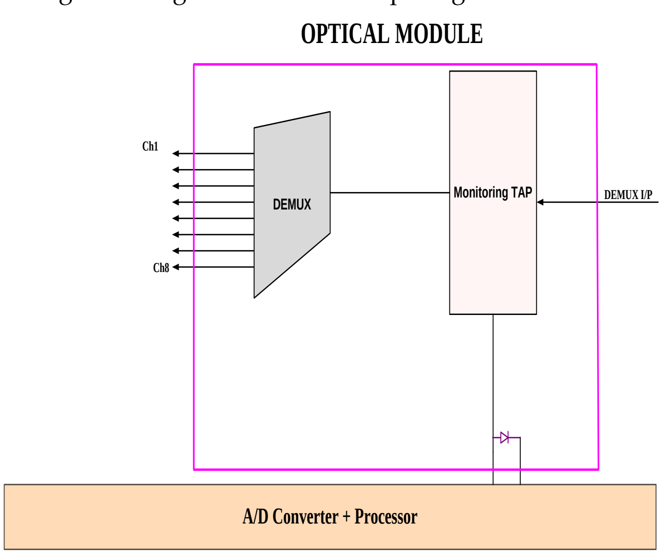

Fig. 4: DEMUX functional schematic

3 DIFFERENT TYPE OF OMD MODULE

3.1 OMD module (Type-1)

Ch1-Ch8 optical Mux input ports with LC/UPC Connector with 50cm optical cables.Ch1-Ch8 optical De-Mux output ports with LC/UPC Connector with 50cm optical cables.Input monitoring tap for monitoring individual channel power channel optical MUX-DEMUX Optical APD diodes. (APD diode leads) Optical Mux Output & Optical Demux Input port with LC/UPC connector with 50cm optical cable. RS232/ I2C Interface is used to communicate with host.

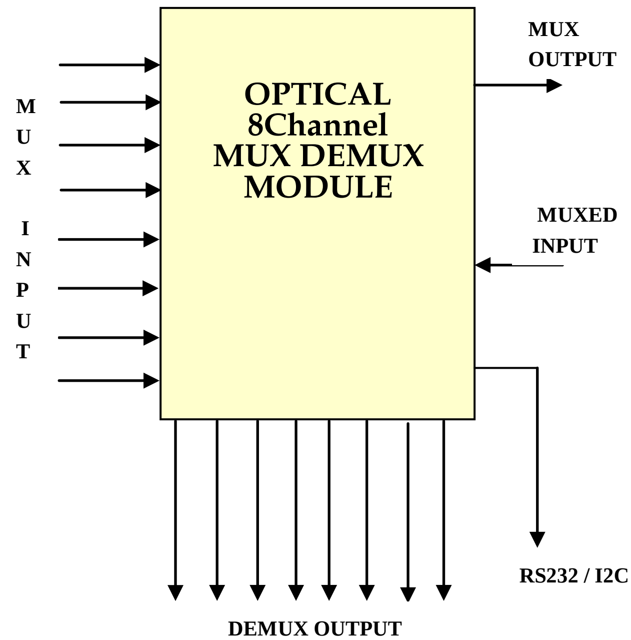

Fig.5: OMD Type-1

3.2 Optical MUX (Type-2)

Ch1 to Ch8-optical input ports with LC/UPC Connector with 50 cm optical cables. Input monitoring tap for monitoring individual channel power.8 channel optical MUX. Optical APD diodes. (APD diode leads). Optical Mux output port with LC/UPC connector with 50 cm optical cable.

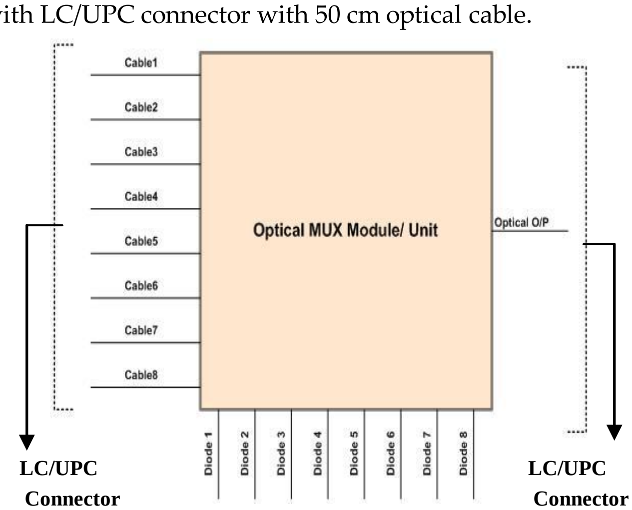

Fig. 6: Optical MUX Type-2

3.3 Optical DEMUX (Type-2)

Optical DEMUX input port with LC/UPC connector with 50 cm optical cable.Input monitoring tap. (APD diode leads).8 channel optical DEMUX.Optical APD diodes. (APD diode leads).Ch1 to Ch8-optical output ports with LC/UPC Connector with 50 cm optical cables.

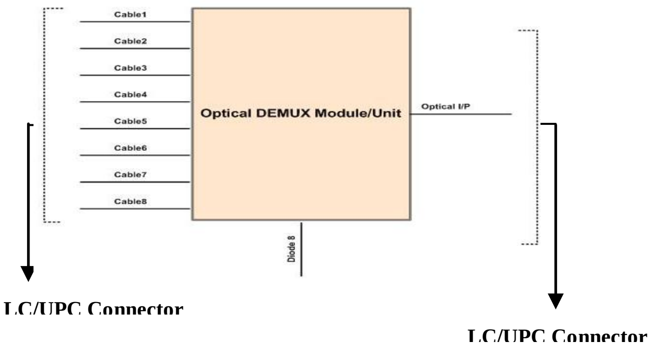

Fig. 7: Optical DEMUX Type-2

3.4 Optical MUX DEMUX integrated module (Type-2)

Ch1-Ch8 optical Mux input ports with LC/UPC Connector with 50cm optical cables.Ch1-Ch8 optical De-Mux output ports with LC/UPC Connector with 50cm optical cables. Input monitoring tap for monitoring individual channel power.8 channel optical MUX-DEMUX.Optical APD diodes. (APD diode leads).Optical Mux Output & Optical Demux Input port with LC/UPC connector with 50cm optical cable.RS232/ I2C Interface is present to interface host.

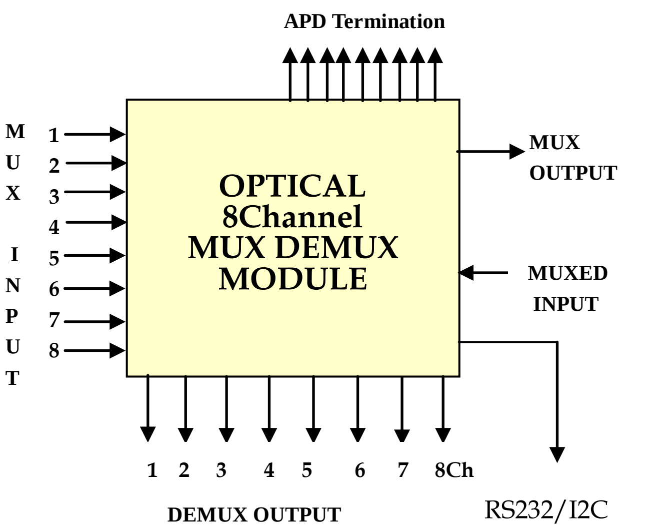

Fig. 8: OpticalMUX DEMUX integrated module Type-2

4 OMD PERFORMANCE REQUIREMENT FOR TYPY1 AND TYPE2 (CWDM)

4.1 wave length allocation

Channel No	Required Wavelength	Unit
λ1	1451	nm
λ2	1471	nm
λ3	1491	nm
λ4	1511	nm
λ5	1531	nm
λ6	1551	nm
λ7	1571	nm
λ8	1591	nm

Table.1: Wave length allocation

4.1 Other parameters

Parameter	Min	Typ	Max	Unit
Channel Spacing		20		nm
Pass band Bandwidth	λN ± 6.5			nm
Variation within Pass band (Ripple)			0.4	dB
Insertion Loss (Single Connector)			2.0	dB
Paired Insertion loss with Connectors	2.0		4.0	dB
Adjacent Channel Isolation	30			dB
Non-Adjacent Channel Isolation	40			dB
Optical Return Loss	45			dB
Directivity	50			dB
Polarization Dependent Loss (PDL)			0.3	dB
Polarization Mode Dispersion (PMD)			0.2	ps
Optical Power Handling			300	mW
Chromatic Dispersion (CD)			±5	ps/nm

Table 2: Other parameters for CDWM

4.2 Monitor, A/D converter performance requirements

Parameter	Min	Typ	Max	Unit
Tributary input power range	-13		7	dBm
Tributary input power meas. accuracy within range			±1	dB
Line input power range	-33		0	dBm
Line input power measurement accuracy within range			±1	dB

Table 3:Monitor,A/D converter performance requirement

5 OMD PERFORMANCE REQUIREMENT FOR TYPY1 AND TYPE2 (DWDM)

5.1 wave length allocation

Channel No	Required Wavelength	Unit
λ1	1528.77	nm
λ2	1529.55	nm
λ3	1530.33	nm
λ4	1531.11	nm
λ5	1531.89	nm
λ6	1532.68	nm
λ7	1533.46	nm
λ8	1534.25	nm

Table.4: Wave length allocation for DWDM

5.2 Other parameters

Parameter	Min	Typ	Max	Unit
Channel Spacing		0.8		nm
Pass band Bandwidth	0.2			nm
Variation within Pass band (Ripple)			0.4	dB
Insertion Loss (Single Connector)			2.0	dB
Paired Insertion loss with Connectors	2.0		4.0	dB
Adjacent Channel Isolation	30			dB
Non-Adjacent Channel Isolation	40			dB
Optical Return Loss	45			dB
Directivity	50			dB
Polarization Dependent Loss (PDL)			0.10	dB
Polarization Mode Dispersion (PMD)			0.1	ps
Optical Power Handling			300	mW
Chromatic Dispersion (CD)			±5	ps/nm

Table 5: Other parameters for DWDM

5 Communication Interface

The communications interface between host (processor or FPGA) and OMD module is through I2C bus. The A/D converters and the EEPROM, holding module specific data, are controlled via the I2C bus and supplied with power from the DC/DC converter.
The I2C bus operates at data rate of 400 kbps with two wires, SCLK and SDA at Open collector, at LVTTL (3.3V).On the I2C bus, host is master, and OMD module is slave, i.e. all communications transactions are initiated by host (master), OMD module (slave) only sends data to host on demand. Viewed from host, OMD module works like an I2C EEPROM, i.e. host can read/write data from/to OMD module at designated address in the EEPROM.

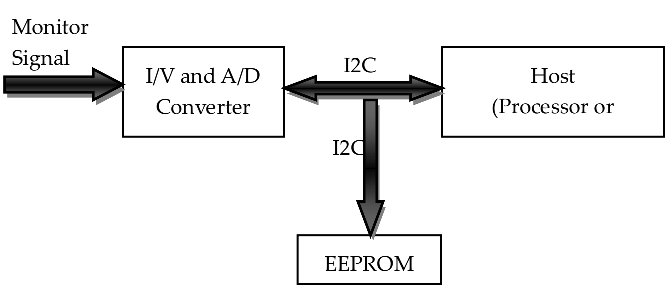

Fig. 9: Communication Interface

5.1 Exrenal Interface Signals

Signal name	I/O	description	level	rate
I2C data	I/O	I2C bidirectional data line	3.3V	<500Khz
I2C clock	I	Clock input to EEPROM from Host	3.3V	<500Khz

Table 6: I2C interface signals

The I2C bus operates at data rate of 400 kbps with two wires, SCLK and SDA at Open collector, at LVTTL (3.3V).On the I2C bus,host is master, and OMD module is slave, i.e. all communications transactions are initiated by host (master),OMD module (slave) only sends data to host on demand.I2C Address On the I2C bus, OMD(slave) is identified by a unique I2C address (7 bit, 0 ~ 127).OMD's I2C slave address is determined in the format of Base Address + Offset ,Let Base Address = 5Ch, or 101 1100 b. Offset = (PosID1 PosID0) b ,For example, if PosID1 = 1, PosID0 = 0, the slave I2C address is 5Eh = 5Ch + 02h = 5Ch + (10) b .Generically, the bit stream on SDA line vs. PosID1 (P1) and PosID0 (P0) is: START 1 0 1 1 1 P1 P0 R/W

6 Higer Order MUX DEMUX

For 88 channels DWDM system two 44 channels MUX are connected through interleaver to get 88 channels as shown below.The host interfacing will remain same (I2C).

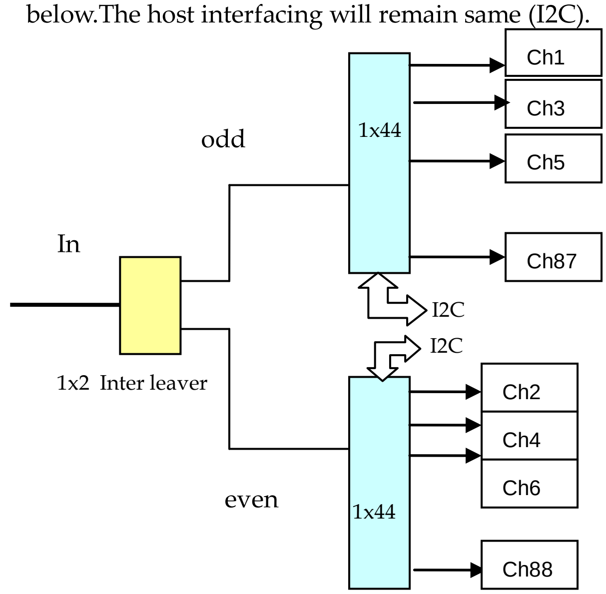

Fig.10:88 channel DEMUX Communication Interface

7 Conclusion

Depending on interface requirement, the communication between host and OMD module may be through RS232.

References

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[2] Product sheets of "CWDM MUX/DEMUX 8; C1."http: //www.transpacket.com/wp-content /uploads /2011 /06/TransPacket-C1-8-Product-sheet-r1.pdf